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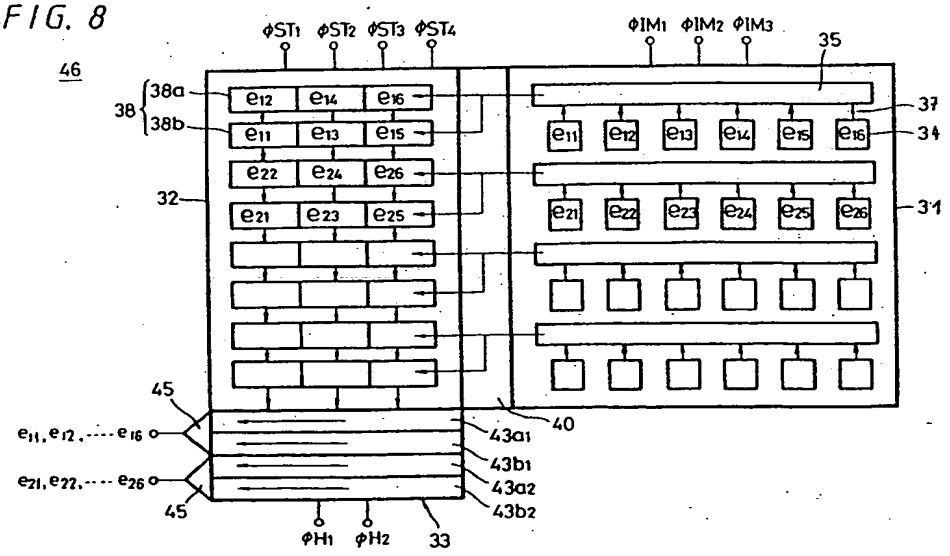
(54) Fit type CCD image sensor.

(57) A charge coupled device image sensor is comprised of an imaging section (31) including a plurality of photoelectric converting sections (34) arrayed in a matrix configuration for generating signal charges and a plurality of horizontal shift registers (35) arranged between the horizontal rows of the photoelectric converting sections (34) for transferring the signal charges via a readout section in the horizontal direction, a storage section having a plurality of horizontal shift registers ($43a_1$ ...) for transferring the signal charges in the horizontal direction and in the vertical direction line by line, a readout section (33) coupled to the storage section and including a plurality of horizontal shift registers for reading out signal charges from the storage section, and a serial-to-parallel converting section (45) provided between the imaging section and the storage section for storing one-line of signal charges from the imaging section into double-line of image signal.

FIG. 8



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Field of the Invention

The present invention generally relates to solid state image sensors and, more particularly, to a solid state image sensor or charge coupled device image sensor of an FIT (frame-interline transfer) type.

Description of the Prior Art

An example of a vertical FIT type solid state image sensor according to the prior art is shown in FIGS. 1 through 3.

Throughout FIGS. 1 to 3, reference numeral 1 designates an image pickup or imaging section, 2 a storage section, and 3 an output section, that is, a horizontal shift register section of a CCD (charge coupled device) structure, respectively. The imaging section 1 is formed of a number of light receiving elements or photoelectric-converting elements 4 arranged in a matrix fashion and a vertical shift register 5 of a CCD structure for transferring signal charges of the light receiving elements 4 in the vertical direction and located on one side of each of vertically arrayed light receiving elements 4. The storage section 2 is located under the imaging section 1 in the vertical direction and adapted to temporarily store the signal charges generated in the imaging section 1. The storage section 2 is comprised of a plurality of vertical shift registers 6 of CCD structure which correspond to the vertical shift registers 5 of the imaging section 1 in a one-to-one relation (1 : 1).

Each of the vertical shift registers 5 and 6 in the imaging section 1 and the storage section 2 employs a 4-phase driving system and is controlled, for example, by 4-phase drive pulses ϕIM_1, ϕIM_2, ϕIM_3, ϕIM_4 and ϕST_1, ϕST_2, ϕST_3, ϕST_4. As shown in FIG. 2, four transfer sections VR (VR_1, VR_2, VR_3, VR_4), each having a transfer electrode are made 1 bit. In the vertical shift register 5 of the imaging section 1, two transfer sections VR_1, VR_2 and two transfer sections VR_3, VR_4 correspond to the light receiving elements 4, respectively. Between each of the light receiving elements 4 and the vertical shift register 5, there is provided a read-out gate section (ROG) 7. In FIG. 2, hatched areas 8 represent channel stop regions. The horizontal shift register 3 of the output section employs, for example, a 2-phase drive system in which it is controlled by 2-phase drive pulses ϕH_1 and ϕH_2. In the horizontal shift register 3, a first storage section st_1, a first transfer section tr_1, a second storage section st_2 and a second transfer section tr_2 form one bit and this 1 bit corresponds to one vertical shift register 6 of the storage section 2.

FIG. 3 is a cross-sectional view taken along the line A - A in FIG. 2. In the horizontal shift register 3, on the surface of a P-type silicon substrate 11 formed is an N-type buried channel layer 12, and transfer electrodes 14 are formed through an insulating film 13 on the buried channel layer 12, thus the respective transfer sections, that is, the first storage section st_1, the first transfer section tr_1, the second storage section st_2 and the second transfer section tr_2 being formed. The transfer electrodes 14 of first storage section st_1 and first transfer section tr_1 are connected commonly to a bus line to which the drive pulse ϕH_1 is applied, while the transfer electrodes 14 of second storage section st_2 and second transfer section tr_2 are commonly connected to a bus line to which the drive pulse ϕH_2 is applied.

In the vertical type FIT solid state imaging element 15, during the vertical blanking period, the signal charges of the light receiving elements 4 are read out to the vertical shift registers 5 through the read-out gate sections 7, transferred through the vertical shift registers 5 and then temporarily stored in the storage section 2. At every horizontal blanking period, the signal charge at every horizontal line is transferred from the storage section 2 to the horizontal shift register section 3. The signal charge of one horizontal line transferred to the horizontal shift register section 3 is transferred in the horizontal direction in the horizontal shift register section 3 and then outputted.

FIG. 4 shows an example of a horizontal type FIT solid state imaging element 16 (described in Japanese Laid-Open Patent Publication No. 61-125077). This horizontal type FIT imaging element 16 is formed such that the storage section 2 is located at one side of imaging section 1 in the horizontal direction and the horizontal shift register section 3 of the output section is located at the lower side of the storage section 2 in the vertical direction. In the imaging section 1, a number of light receiving elements 4 are arrayed in a matrix configuration and at one side of each row of horizontally-arrayed light receiving elements 4, there is located a horizontal shift register 17 which corresponds to the vertical shift register 5 of the former example. The horizontal shift register 17 can employ a 3-phase drive system which is controlled, for example, by 3-phase drive pulses ϕIM_1, ϕIM_2 and ϕIM_3 shown in FIG. 4. In this case, as shown in FIG. 5, three transfer sections VR (VR_1, VR_2, VR_3), each having a transfer electrode, are made as 1 bit and this 1 bit corresponds to each light receiving element 4. The signal charge from each of the light receiving elements 4 is transferred to the horizontal shift register 17 through the read-out gate section (ROG) 7, transferred in the horizontal direction and then stored in the storage section 2 temporarily.

The storage section 2 comprises a plurality of horizontal shift registers 18 which correspond to the horizontal shift registers 17 in the imaging section 1 at one-to-one relation (1 : 1). The adjacent horizontal shift registers 18 are coupled through a gate section (transfer channels SR_5 controlled by a gate electrode) 19 for transferring the signal charge in the vertical direction as shown in FIG. 5. Each of the horizontal shift registers 18 employs, for example, a 4-phase drive system which is controlled by 4-phase drive pulses ϕST_1, ϕST_2, ϕST_3, ϕST_4 and in which four transfer sections SR (SR_1, SR_2, SR_3, SR_4) are made as 1 bit and two transfer sections SR_2, SR_1 in the upper horizontal shift registers 18 are coupled through the gate section 19 to two transfer sections SR_4, SR_3 in the adjacent lower horizontal shift register 18. Since the respective transfer sections SR_1, SR_2, SR_3, SR_4 of each of the horizontal shift registers 18 are respectively formed in correspondence to one another in the vertical direction, the gate section 19 is formed in a slant direction in order to couple the transfer sections which are displaced each other by a half bit. In the storage section 2, the vertical transfer of the signal charge to the output side thereof (to the horizontal shift register section 3) is carried out in a so-called zigzag fashion in which the charges in the transfer sections SR_2, SR_1 are transferred to the transfer sections SR_4, SR_3 by a half bit in the horizontal direction and then transferred to the transfer sections SR_2, SR_1 of the lower stage of the horizontal shift register 18.

The horizontal shift register section 3 of the output section is formed of two horizontal shift registers, namely, a first horizontal shift register 20 and a second horizontal shift register 21. The first and second horizontal shift registers 20 and 21 are coupled through a gate section (i.e., a transfer channel controlled by a gate electrode) 22. Each of the first and second horizontal shift registers 20 and 21 employ, for example, 2-phase drive system which is controlled by 2-phase drive pulses ϕH_1 and ϕH_2. In this case, a first storage section st_1, a first transfer section tr_1, a second storage section st_2 and a second transfer section tr_2 form one bit which corresponds to one bit of the horizontal shift register 18 of the storage section 2. The second storage and transfer sections st_2 and tr_2 of the first horizontal shift register 20 are coupled to the first storage and transfer sections st_1 and tr_1 of the second horizontal shift register 21 through the gate section 22. In that case, the corresponding storage and transfer sections of the first and second horizontal shift registers 20 and 21 are formed to correspond to one another in the vertical direction so that the gate section 2 is formed to be inclined.

In the horizontal shift register section 3, there is line-transferred the signal charge of the horizontal line from the storage section 2. That is, signal charges of the light receiving elements 4 on, for example, an odd horizontal line are transferred to the first horizontal shift register 20, while the signal charges of the light receiving elements 4 on an even horizontal line are transferred to the second horizontal shift register 21. Then, these signal charges are transferred at the same time in the horizontal direction so that the signal charges of two horizontal lines are outputted simultaneously.

In the horizontal type FIT solid state imaging elements 16, since the horizontal pitch (i.e., one bit distance) of the horizontal shift registers 18 in the storage section 2 does not depends on the light receiving system, the horizontal pitch 16 can be designed freely. Thus, the horizontal pitch of the horizontal shift register section 3 at the output section can be designed with a room. Therefore, even when the imaging section 1 is made high in image density, the horizontal shift registers 20 and 21 of the output section can be formed. Thus, it is possible to make the FIT type solid state imaging element with high image density.

In the vertical type FIT solid state imaging element 15, as shown in FIG. 6, a width W_1 of one pixel (one cell) a of the imaging section 1 corresponds to a transfer channel width W_2 of the vertical shift register 6 in the storage section 2 and then a horizontal pitch (i.e., length of one bit) X_1 of the horizontal shift register section 3 at the output section is determined correspondingly. Therefore, if the number of pixels, particularly the number of pixels in the horizontal direction is increased, then the length X_1 of one bit in the horizontal shift register section 3 is reduced, which requires a fine pattern technique. Further, the transfer channel width W_2 of the vertical shift register 6 is reduced so that various problems such as the deterioration of transfer efficiency or the like occur.

In the horizontal type FIT solid state imaging element 16, if as shown in FIG. 7 the area of one pixel (one cell) a in the imaging section 1 is selected to be the same as that of FIG. 6, then a horizontal pitch (i.e., one bit length) P of the horizontal shift registers 18 in the storage section 2 can be increased so that a horizontal pitch (one bit length) X_2 of the horizontal shift register section 3 at the output section can also be increased. Thus, the solid state imaging element 16 can be made high in pixel density. However, when the horizontal pitch P of the horizontal shift registers 18 in the storage section 2 is selected to be long, then the chip size of the whole solid state imaging element becomes large and the ratio between the width W and the length L of the horizontal shift register 18 is reduced so that the transfer efficiency of the storage section 2 in the frame transfer (i.e., when

the signal charge is transferred from the imaging section 1 to the storage section 2) is lowered.

On the other hand, when the horizontal pitch P in the storage section 2 is selected to be small, then the ratio between the width W and the length L in the frame transfer is increased. However, the ratio between the width W and the length L of the transfer channel during a so-called line transfer in which the signal charge is transferred from the imaging section 2 to the horizontal shift register section 3 is reduced (in an inverse proportion fashion) and hence the transfer efficiency is lowered. Further, when the density of pixels is increased, then the number of pixels in the horizontal direction is increased so that the frame transfer frequency in the storage section 2 and the horizontal transfer frequency in the horizontal shift register section 3 are increased, which needs large electric power.

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a solid state image sensor which can eliminate the disadvantages encountered with the prior art.

It is another object of the present invention to provide a solid state image sensor whose chip size can be reduced when a density of pixels is increased.

It is a further object of the present invention to provide a solid state image sensor in which the horizontal transfer frequency of a horizontal shift register section and the frame transfer frequency of a storage section can be lowered.

According to an aspect of the present invention, a charge coupled device image sensor is comprised of an imaging section including a plurality of photoelectric converting sections arrayed in a matrix configuration for generating signal charges and a plurality of horizontal shift registers arranged between the horizontal rows of the photoelectric converting sections for transferring the signal charges via a readout section in the horizontal direction, a storage section having a plurality of horizontal shift registers for transferring the signal charges in the horizontal direction and in the vertical direction line by line, a readout unit coupled to the storage section and including a plurality of horizontal shift registers for reading out signal charges from the storage section, and a serial-to-parallel converter provided between the imaging section and the storage section for storing one-line of signal charges from the imaging section into double-line of signal charges.

The above and other objects, features, and advantages of the present invention will become apparent from the following detailed description of an illustrative embodiment thereof to be read in conjunction with the accompanying drawings, in which like reference numerals are used to identify the same or similar parts in the several views.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view illustrative of a structure of an example of a conventional vertical type FIT solid state imager;

FIG. 2 is a plan view illustrative of a main portion of FIG. 1;

FIG. 3 is a cross-sectional view taken through the line A - A in FIG. 2;

FIG. 4 is a plan view illustrative of a structure of an example of a conventional horizontal type FIT solid state image sensor;

FIG. 5 is a plan view of a main portion of FIG. 4;

FIG. 6 is an explanatory diagram of FIG. 1;

FIG. 7 is an explanatory diagram of FIG. 4;

FIG. 8 is a plan view illustrative of a structure of an embodiment of a horizontal type FIT solid state image sensor according to the present invention;

FIG. 9 is a plan view of a main portion of FIG. 8; and

FIG. 10 is a plan view illustrating another embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

An embodiment of a horizontal type FIT solid state image sensor 46 according to the present invention will be described with reference to FIGS. 8 and 9.

In the figures, reference numeral 31 denotes an imaging section, 32 a storage section which temporarily stores the signal charges from the imaging section 31 and is located at one side of the imaging section 31 in the horizontal direction, and 33 a horizontal shift register section of an output section which is located under the storage section 32. The image section 31 is formed of a number of imaging or light receiving elements 34 arrayed in a matrix configuration and a horizontal shift register 35 of a CCD structure located on one side of each of the rows of horizontally-arranged light receiving elements 34 for transferring the signal charges from the light receiving elements 34 to the storage section 32. A read-out gate (ROG) 37 is provided between each of the light receiving elements 34 and the horizontal shift register 35 for reading out the signal charge from each light receiving element 34 and transferring the same to the horizontal shift register 35. Each of the horizontal shift registers 35 employs, for example, a 3-phase drive system which is controlled by 3-phase drive pulses ϕIM_1, ϕIM_2, ϕIM_3 and in which three transfer sections VR

(VR_1, VR_2, VR_3), each having a transfer electrode, are made as one bit and this one bit corresponds to each light receiving element 34.

In the storage section 32, a plurality of cells (i.e., two cells b_1, b_2 in this embodiment) corresponds to one pixel (one cell) a of the imaging section 31 in the vertical direction. Accordingly, in order that the light receiving elements 34 arranged in one horizontal line (row) of the imaging section 31 correspond with a plurality of horizontal shift registers, in this embodiment, two horizontal shift registers 38a, 38b, a plurality of the horizontal shift registers 38 are provided. Therefore, the number of cells of each horizontal shift register 38 in the horizontal direction is 1/2 of the number of light receiving elements 34 of each horizontal line in the imaging section 31 in the horizontal direction. The signal charges of one horizontal line in the imaging section 31 are stored through a serial-to-parallel converting section 40, which will be described later, in two horizontal shift registers 38a, 38b in a divided condition. That is, the signal charges at every other light receiving elements 34 of one horizontal line are stored in the first horizontal shift register 38a, while the signal charges at the remaining every other light receiving elements 34 of the same horizontal line are stored in the second horizontal shift register 38b.

Each of the horizontal shift registers 38 employs, for example, a 4-phase drive system which is controlled by 4-phase drive pulses ϕST_1, ϕST_2, ϕST_3, ϕST_4 and in which four transfer sections SR (SR_1, SR_2, SR_3, SR_4), each having a transfer electrode, are made as one bit. The adjacent horizontal shift registers 38 (38a, 38b) in the vertical direction are coupled through a gate section (i.e., a transfer channel SR_5 controlled by a gate electrode to which an independent gate voltage is applied) 39. This gate section 39 is formed between two transfer sections SR_2 and SR_1 forming a half bit of the upper horizontal shift register 38a and two transfer sections SR_4, SR_3 forming a half bit of the lower horizontal shift register 38b. Since the respective transfer sections SR_1, SR_2, SR_3, SR_4 of each horizontal shift register 38 are formed in correspondence with one another in the vertical direction, the gate section 39 is inclined so as to couple the transfer sections which are displaced by a half bit.

In the serial-to-parallel converting section 40, as shown in FIG. 9, transfer sections VR_1 and VR_2 are so provided in the vertical direction that they correspond to two horizontal shift registers 38a, 39b in the storage section 32, and a gate section (i.e., a transfer channel α controlled by a gate electrode to which an independent gate voltage is applied) is provided between the transfer section VR_2 which corresponds to the first horizontal shift register 38a and the transfer section VR_1 which corresponds to the second horizontal shift register 38b.

Further, the transfer section VR_1 corresponding to the first horizontal shift register 38a at the upper stage is coupled to the last stage of transfer section VR_3 of the horizontal shift register 35 in the imaging section 31. At the former stages of the first and second horizontal shift registers 38a, 38b in the storage section 32, which former stages contact with the serial-to-parallel converting section 40, gate sections β are formed, respectively.

In the horizontal shift register section 33 of the output section, there are provided two sets of horizontal shift registers one set of which is formed of two horizontal shift registers 43a, 43b, that is, totally four horizontal shift registers 43 (43_{a1}, 43_{b1}, 43_{a2}, 43_{b2}) in correspondence with the first and second horizontal shift registers 38a, 38b in the storage section 32.

Each of the four horizontal shift registers 43 employs a 2-phase drive system which is controlled by 2-phase drive pulses ϕH_1, ϕH_2 and in which four transfer sections, namely, a first storage section st_1, a first transfer section tr_1, a second storage section st_2 and a second transfer section tr_2 form one bit. In this case, the storage section st_1, the transfer section tr_1, the storage section st_2 and the transfer section tr_2 are so formed that they correspond to the transfer sections SR_1, SR_2, SR_3 and SR_4 in the storage section 32, respectively.

The adjacent horizontal shift registers 43 in the vertical direction are coupled by a gate section (i.e., a transfer channel γ which is controlled by a gate electrode supplied with an independent gate voltage) 44. That is, the second storage section st_2 and the second transfer section tr_2 of the upper stage of horizontal shift register 43 are coupled to the first storage section st_1 and the first transfer section tr_1 of the lower stage of horizontal shift register 43 by the gate section 44.

At the last stage of the horizontal shift register section 33, there is provided a serial-to-parallel converting section 45 of an inverse conversion type relative to the serial-to-parallel converting section 40 to return the signal charges of each set of horizontal shift registers 43a, 43b to the signal charges of one horizontal line. In the illustrated embodiment, the above conversion is carried out by switching means. The transfer sections SR_4, SR_3 of the lowermost horizontal shift register 38 in the storage section 32 are coupled to the first storage section st_1 and the first transfer section tr_1 of the uppermost horizontal shift register 43 in the horizontal shift register section 33 through the gate section 39. In FIG. 9, a hatched area 48 is a channel stopper region.

Operation of the solid state image sensor 46 will be described below.

During the vertical blanking period, the signal charges from all the light receiving elements 34 of the imaging section 31 are transferred to the horizontal shift registers 35 through the read-out gate sections 37 (all pixels are read out), transferred through the horizontal shift registers 35 to the storage section 32 and then temporarily stored therein. At that time, the signal charges transferred through the horizontal shift registers 35 in the imaging section 31 are divided by the serial-to-parallel converting section 40 into the signal charges of every other light receiving elements (odd-numbered elements) 34 of one horizontal line and into the signal charges of remaining every other light receiving elements (even-numbered elements) 34 of the same horizontal line. By way of example, the signal charges of odd-numbered light receiving elements 34 are transferred through the gate section 41 to the lower stage transfer section VR_2, while the signal charges of the even-numbered light receiving elements 34 are transferred to the upper stage transfer section VR_2. Then, both signal charges are transferred at the same time through the gate sections 42 (β) to the corresponding horizontal shift registers 38a and 38b in the storage section 32, respectively. The above transfer of signal charges is repeated so that the signal charges are transferred to the storage section 32 in a so-called frame transfer fashion.

At the completion of the frame transfer of signal charges, the signal charges of the light receiving elements 34 on each horizontal line or row are distributed to the first and second horizontal shift registers 38a and 38b in the storage section 32. The signal charge of the odd-numbered light receiving elements 34 on the horizontal line are sequentially stored in the respective cells of the second horizontal shift registers 38b, while the signal charges of the even-numbered light receiving elements 34 on the same horizontal line are sequentially stored in the respective cells of the first horizontal shift register 38a. That is, as shown in FIG. 8, as to the signal charges e_{11} to e_{16} of one horizontal line, odd-numbered signal charges e_{11}, e_{13}, e_{15} are stored in the second horizontal shift register 38b, while the even-numbered signal charges e_{12}, e_{14}, e_{16} are stored in the first horizontal shift register 38a.

Then, at every horizontal blanking period, the signal charges of two horizontal lines are transferred from the storage section 32 to the horizontal shift register section 33 at the output section in a line transfer fashion in which the signal charges of the first and second horizontal shift registers 38a and 38b are taken as the signal charges of one horizontal line. In the storage section 32, the signal charges of the transfer sections SR_2, SR_1 are transferred to the transfer sections SR_4, SR3 by a half bit in the horizontal direction and then transferred to the transfer sections SR_2, SR_1 of the lower stage horizontal shift register 38 through the transfer channel SR_5 of the gate section 39 in a zigzag fashion in the vertical direction. In the horizontal shift register 33, after the signal charge of the first storage section st_1 is transferred to the second storage section st_2 by a half bit in the horizontal direction, the signal charge is transferred through the transfer channel γ of the gate section 44 to the first storage section st_1 of the horizontal shift register 43 at the lower stage in a zigzag fashion in the vertical direction. As a result, in the storage section 32, the signal charges of the first and second horizontal shift registers 38a, 38b corresponding to one horizontal line (e.g., the even-numbered horizontal line) are transferred to the third and fourth horizontal shift registers 43_{a2}, 43_{b2} in the output section. The signal charges of the first and second horizontal shift registers 38a and 38b corresponding to the next one horizontal line (e.g., the odd-numbered horizontal line) are transferred to the first and second horizontal shift registers 43_{a1} and 43_{b1} at the output section, respectively.

In the horizontal shift register section 33, the signal charges in the first to fourth horizontal shift registers 43_{a1} to 43_{b2} are transferred in the horizontal direction, and then from the first serial-to-parallel converting section 45, there are alternately delivered the signal charges of the first and second horizontal shift registers 43_{a1} and 43_{b1}, while from the second serial-to-parallel converting section 45, there are alternately delivered the signal charges of the third and fourth horizontal shift registers 43_{a2} and 43_{b2}. Thus, the signal charges of the odd- and even-numbered horizontal lines are simultaneously delivered in the order of the signal charges on one horizontal line in the imaging section 31. More specifically, as shown in FIG. 8, the signal charges are delivered from the one output in the order of e_{11}, e_{12}, ..., e_{16}, while from the other output in the order of e_{21}, e_{22}, ..., e_{26}, respectively.

According to the horizontal type FIT solid state image sensor 46 having the above-mentioned structure, one pixel (cell) a of the imaging section 31 corresponds to a plurality of cells arranged in the vertical direction in the storage section 32, or two cells b1 and b2 in this embodiment (see FIG. 9) and the serial-to-parallel converting section 40 is provided between the imaging section 31 and the storage section 32, whereby the signal charges on one horizontal line of imaging section 31 are stored in the two horizontal shift registers 38a and 38b in the divided state. Thus, the number of cells of the storage section 32 in the horizontal direction can be reduced to 1/2 of the number of cells of the prior-art horizontal FIT solid state image sensor 16 shown in FIG. 4. Therefore, since the total length of

the storage section 32 in the horizontal direction can be reduced as compared with the prior-art example shown in FIG. 4, the total chip size of the solid state image sensor of the present invention can be reduced. Further, since the number of cells of the storage section 32 becomes 1/2, the length of each cell in the horizontal direction can be increased on the contrary, which means that the horizontal length of the cell of the horizontal shift register section 33 at the output section can be increased. As a result, the fine pattern technique for the transfer electrode and so on of the horizontal shift register section 33 and the storage section 32 can be avoided.

Also, the ratio between the width W of the transfer section and its length L upon line transfer becomes twice as large as that of the prior-art example shown in FIG. 4, so that the transfer efficiency can be improved. Although the cell size of the storage section 32 in the horizontal direction is not dependent on the optical system, the freedom in its vertical direction is increased. Further, the horizontal transfer frequency in the horizontal shift register section 33 and the frame transfer frequency in the storage section 32 can be reduced to 1/2 of those of the prior-art example shown in FIG. 4. As a consequence, the transfer efficiency can be improved and also the amount of signal charges processed can be increased.

As set forth above, since the freedom of designing the storage section 32 and the horizontal shift register section 33 at the output section can be improved both in the horizontal and vertical directions, it is possible to obtain the optimum cell size of the storage section in view of the transfer efficiency, the amount of processed signal charges, the accuracy of the fine pattern technique and the chip size. Thus, the high pixel density can be promoted in this kind of solid state image sensor.

In the embodiment of the present invention shown in FIGS. 8 and 9, although one storage section 32 is disposed at one side of the imaging section 31 in the horizontal direction, the storage section 32 may be provided at both sides imaging section 31. This example is shown in FIG. 10.

In this example, first and second storage sections 32A and 32B are located at both sides of the imaging section 31 in the horizontal direction, and first and second horizontal shift register sections 33A and 33B of the output section are respectively located beneath the first and second storage sections 32A and 32B. The imaging section 31 of this embodiment comprises the eight receiving elements 34 the number of which is the same as that of the imaging section 31 shown in FIG. 8 and the horizontal shift registers 35 corresponding to respective horizontal rows of the light receiving elements 34 (in FIG. 10, for the sake of explanation the number of light receiving elements 34 on each horizontal row is 8)).

In this embodiment, the first storage section 32A comprises two cells in the vertical direction for one pixel (one cell) of the imaging section 31 and four horizontal shift registers 38 (38a, 38b, 38c, 38d) for each of odd-numbered horizontal lines in the imaging section 31. A first serial-to-parallel converting section 40A is provided between the first storage section 32A and the imaging section 31. The second storage section 32B comprises four horizontal shift registers 38 (38a, 38b, 38c, 38d) for each of even-numbered horizontal lines symmetrical with respect to the first storage section 32A and a second serial-to-parallel converting section 40B is provided between the second storage section 32B and the imaging section 31.

Each of the first and second horizontal shift register sections 33A and 33B at the output section has four horizontal shift register sections 43 (43a, 43b, 43c, 43d) corresponding to the four horizontal shift registers 38 of each of the first and second storage sections 32A and 32B and whose structure is similar to that shown in FIG. 9A. At the final stages of the horizontal shift register sections 33A, 33B, there are respectively provided serial-to-parallel converting sections of inverse conversion type (e.g., switching means similar to those of FIG. 9) 45A, 45B to return the signal charges from the horizontal shift register 43a through 43d to the signal charges of one horizontal line and then deliver the same.

In the imaging section 31, except for the fact that the averaging order of the transfer sections VR_1 to VR_3 of the horizontal shift registers 35 on the odd- and even-numbered horizontal lines are inverted to transfer the signal charges in the opposite directions, its remaining structure is substantially the same as that of the imaging section 31 shown in FIG. 9.

Even in the first and second storage sections 32A and 32B, the averaging order of the transfer sections SR_1 to SR_4 of each of the horizontal shift registers 38 is inverted to transfer the signal charges in the opposite directions in the horizontal direction and the remaining structure thereof is substantially the same as that of the storage section 32 shown in FIG. 9. In the serial-to-parallel converting sections 40A and 40A, which divide the signal charges of the light receiving elements 34 on one horizontal line in the imaging section 31 into four horizontal shift registers 38a to 38d of each of the storage sections 32A and 32B, the transfer sections VR_1, VR_2 are made as 1 cell and the cell number thereof is increased to 4 and the transfer sections VR_1, VR_2 are arranged so as to transfer the signal charges in the opposite directions vertically. The remaining structure thereof is

substantially the same as that of serial-to-parallel converting section 40 shown in FIG. 9.

According to the horizontal FIT type solid state image sensor 47 arranged as above, during the vertical blanking period, the signal charges of the light receiving elements 34 of the odd-numbered horizontal lines in the imaging section 31 are read out to the horizontal shift register 35, transferred to the left-hand side horizontally as shown in FIG. 10 and then respectively transferred to the four horizontal shift registers 38a to 38d of the first storage section 32A through the serial-to-parallel converting section 40A in a divided form so as to be stored therein. The signal charges e_{11} to e_{18} of the odd-numbered horizontal lines, for example, are stored in the first to fourth horizontal shift registers 38a to 38d as shown in FIG. 10. Simultaneously, the signal charges of the light receiving elements on the even-numbered horizontal lines in the imaging section 31 are read out to the horizontal shift register 35, horizontally transferred to the right-hand side of FIG. 10, respectively transferred through the second serial-to-parallel converting section 40B to the corresponding four horizontal shift registers 39a to 38d of the second storage section 32B in a divided form and then stored therein. The signal charges e_{21} to e_{28} of the even-numbered horizontal lines, for example, are respectively stored in the first to fourth horizontal shift registers 38a to 38d as shown in FIG. 10.

Next, during the horizontal blanking period, the signal charges of the four horizontal shift registers 38a to 38d of the respective storage sections 32A and 32B are respectively transferred to the four horizontal shift registers 43a to 43d of the first and second horizontal shift register sections 33A and 33B. Then, the signal charges are simultaneously transferred within the respective horizontal shift registers 43a to 43d, alternately outputted from the serial-to-parallel converting sections 45A and 45B, outputted from the first horizontal shift register section 33A in the order of the signal charges on the odd-numbered horizontal lines in the imaging section 31 and then simultaneously outputted from the second horizontal shift register section 33B in the order of the signal charges on the even-numbered horizontal shift register. More specifically, the first horizontal shift register section 33A outputs the signal charges e_{11} to e_{18} of the odd-numbered lines and the second horizontal shift register section 33B outputs the signal charges e_{21} to e_{28} of the even-numbered lines, respectively.

According to the horizontal FIT type solid state image sensor element 47 thus arranged, the horizontal transfer frequencies of the horizontal shift register sections 33A, 33B and the frame transfer frequencies of the storage sections 32A, 32B are lowered to 1/2 as compared with those of the solid state imaging element 46 of FIG. 8, accordingly, 1/4 as compared with those of the conventional solid state image pickup element of FIG. 4, thereby the transfer efficiency being increased and the amount of signal charges to be treated being increased. Further, since the storage sections 32A and 32B are symmetrically provided with respect to the imaging section 31, the center of the chip constructing the solid state image sensor element can be made closer to the optical center.

While the two horizontal shift registers 38a, 38b are provided in the storage section 32 for the light receiving element of one horizontal line so as to allow the two cells to vertically correspond to one pixel (one cell) of the imaging section 31 as shown in FIG. 8, a plurality of horizontal shift registers, for example, more than two horizontal shift registers are provided in one pixel (one cell) in a divided form such that a plurality of cells, for example, more than two cells correspond vertically to one pixel (one cell). Simultaneously, the horizontal shift registers the number of which corresponds to the number of the divided horizontal shift registers are provided in the horizontal shift register section 33. According to the above-mentioned arrangement, the width W/lenght L of the transfer section upon line transfer is increased to become several times the divided number of more than 2 and the horizontal transfer frequency of the horizontal shift register section and the frame transfer frequency of the storage section can be reduced to 1/divided number as compared with those of the prior art. Furthermore, if the similar divided number is provided in FIG. 10, then the horizontal transfer frequency and the frame transfer frequency are reduced to 1/(divided number x 2) as compared with those of FIG. 8.

According to the solid state image sensor of the present invention, the fine pattern technique of the horizontal shift register section in the output section, the transfer electrodes of the storage section or the like are not needed and the entire chip size constructing the solid state image sensor can be reduced. Also, the transfer efficiency upon line transfer can be increased. Further, the horizontal transfer frequency of the horizontal shift register section and the frame transfer frequency of the storage section can be reduced. Furthermore, the transfer efficiency can be increased and the amount of signal charges to be processed can be optimized. In addition, the cell size of the storage section in the horizontal and vertical directions can be increased in freedom and the design of the same can be optimized with ease. Therefore, the density of pixels in the solid state image sensor can be increased more.

Having described the preferred embodiment of the invention with reference to the accompanying

drawings, it is to be understood that the invention is not limited to that precise embodiment and various changes and modifications thereof could be effected by one skilled in the art without departing from the spirit or scope of the invention as defined in the appended claims.

Claims

1. A charge coupled device image sensor comprising:
   (a) an imaging section (31) including a plurality of photoelectric converting sections (34) arrayed in a matrix configuration for generating signal charges and a plurality of horizontal shift registers (35) arranged between the horizontal rows of the photoelectric converting sections for transferring the signal charges via a readout section in the horizontal direction;
   (b) a storage section (32) having a plurality of horizontal shift registers (38a, 38b) for transferring the signal charges in the horizontal direction and in the vertical direction line by line;
   (c) readout means (33) coupled to said storage section and including a plurality of horizontal shift registers ($43a_1$...) for reading out signal signal charges from said storage section; and
   (d) serial-to-parallel converting means (45) provided between said imaging section and said storage section for storing one-line of signal charges from said imaging section into double-line of signal charges.

2. A charge coupled device image sensor according to claim 1, in which each of the plurality of said horizontal shift registers of said storage section includes a gate portion at an input side thereof.

3. A charge coupled device image sensor according to claim 2, in which said serial-to-parallel converting means includes a pair of transfer sections coupled to each output of the plurality of said horizontal shift registers of said imaging section and a channel provided between the pair of said transfer sections and controlled by a gate voltage.

4. A charge coupled device image sensor according to claim 2, in which the pair of transfer sections of said serial-to-parallel converting means are coupled to corresponding gate portions of said storage section.

5. A charge coupled device image sensor according to claim 1, in which said storage section is divided into two portions and said two portions are provided at both sides of said imaging section.

Fig 1 (prior art)

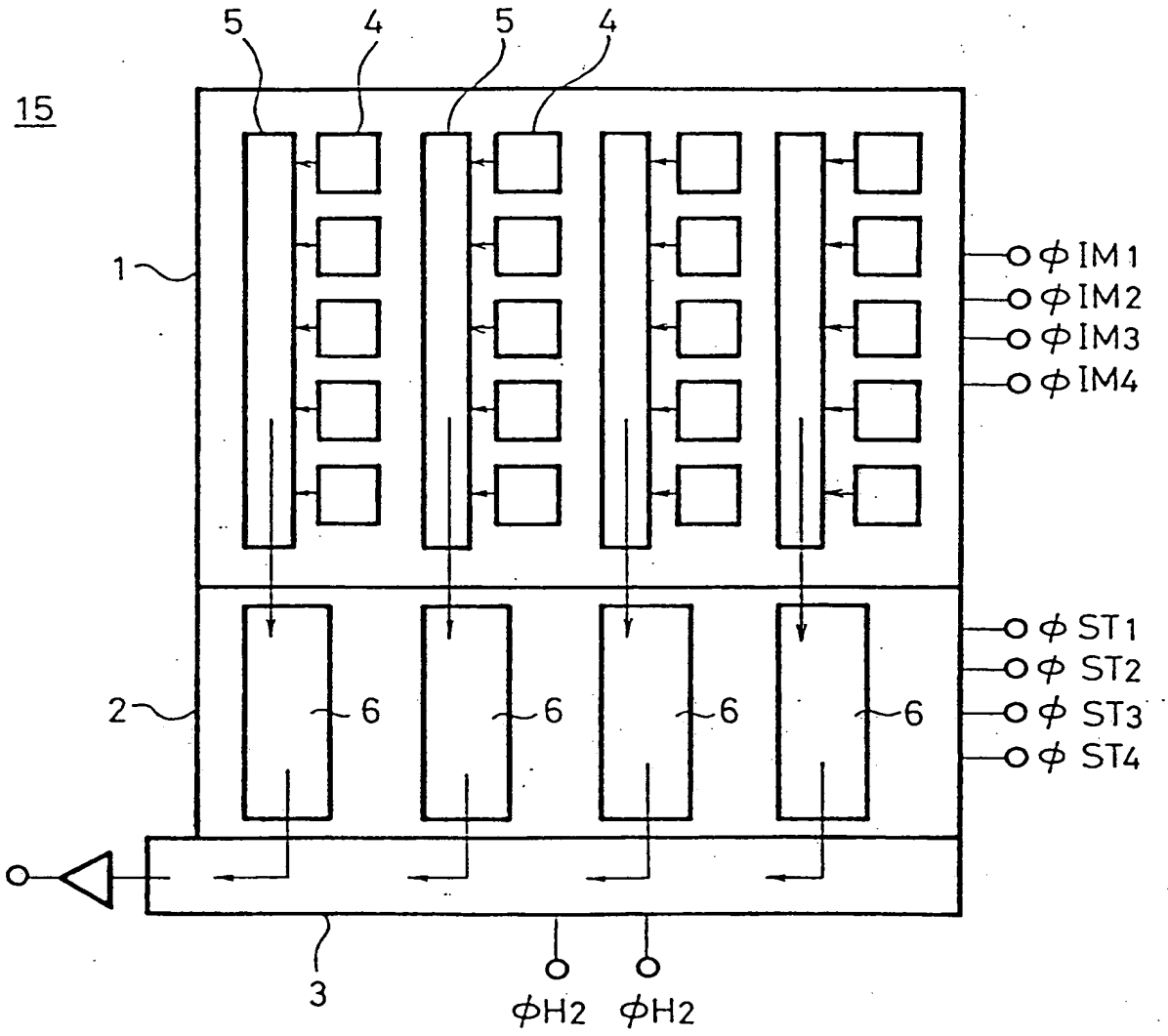


Fig. 2 (prior art)

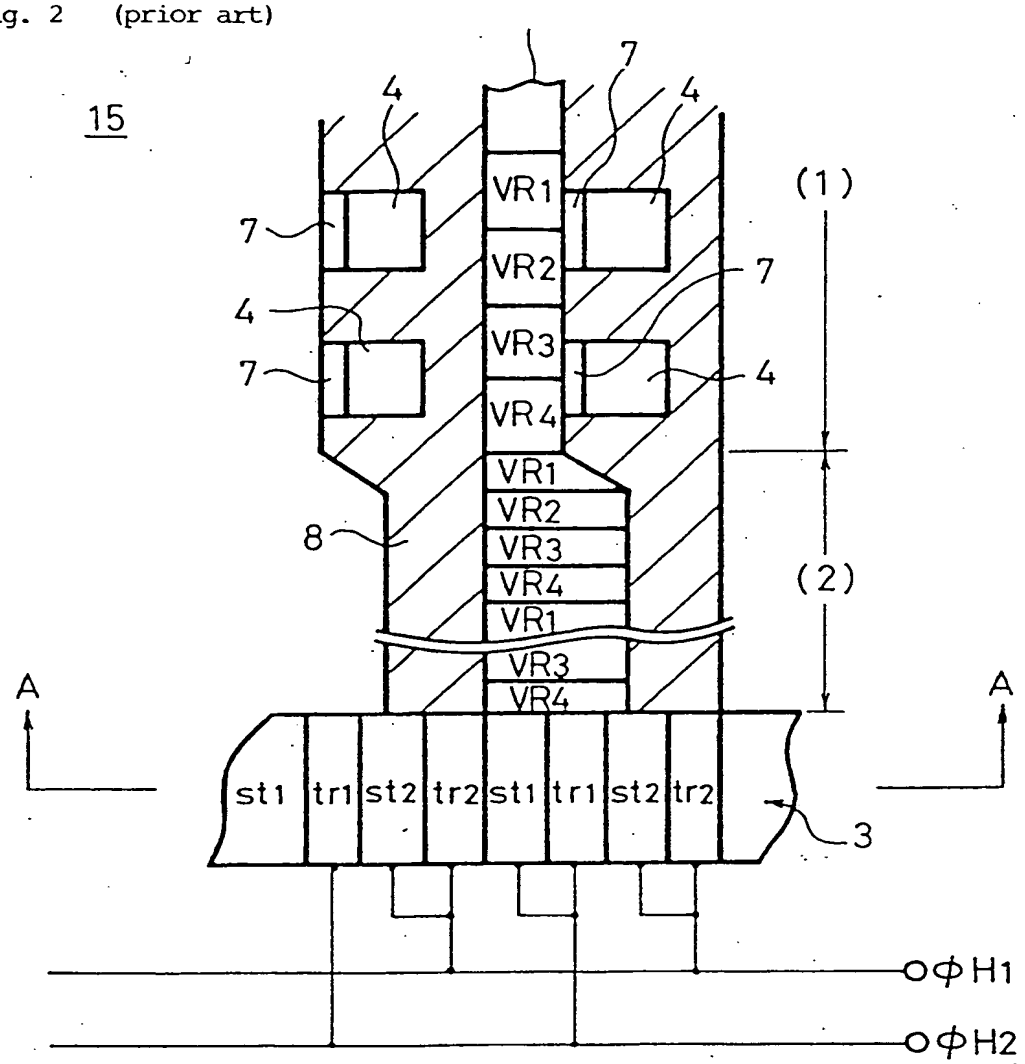
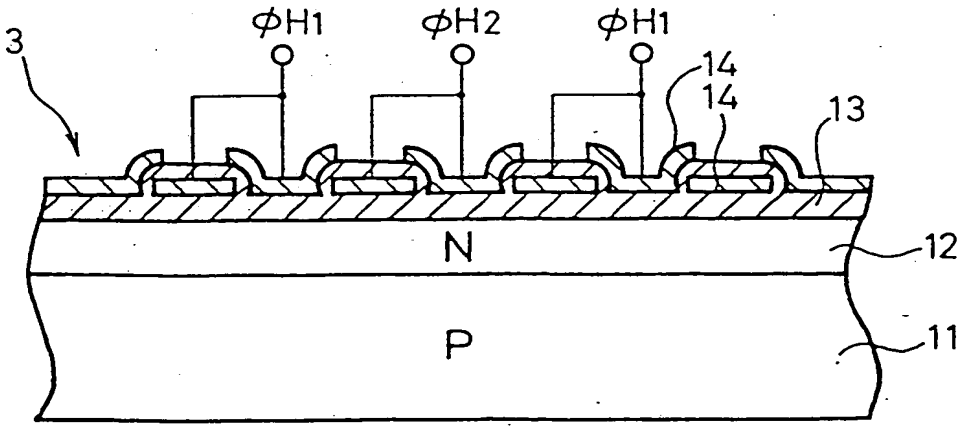


FIG. 3 (PRIOR ART)



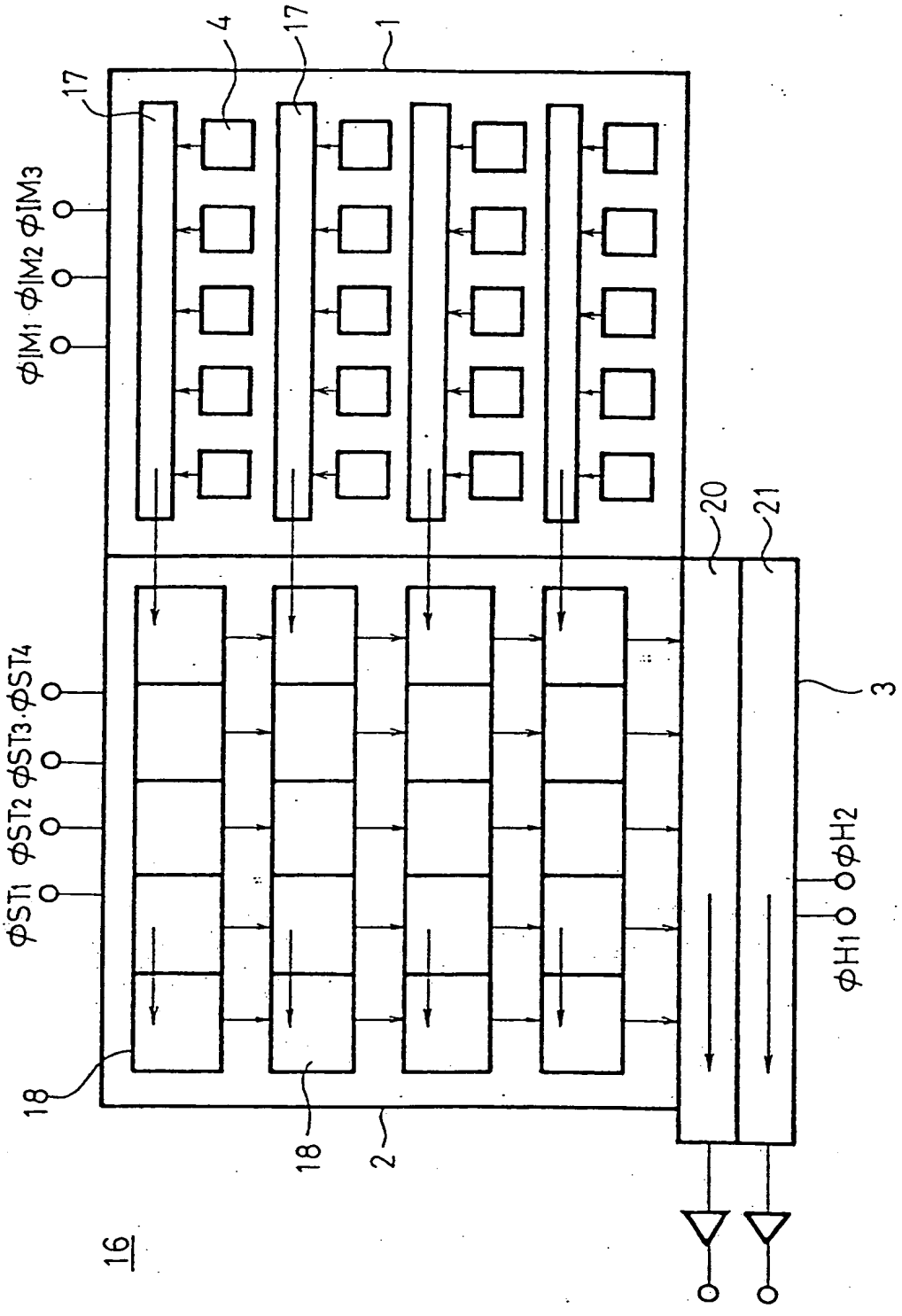


FIG. 4 (PRIOR ART)

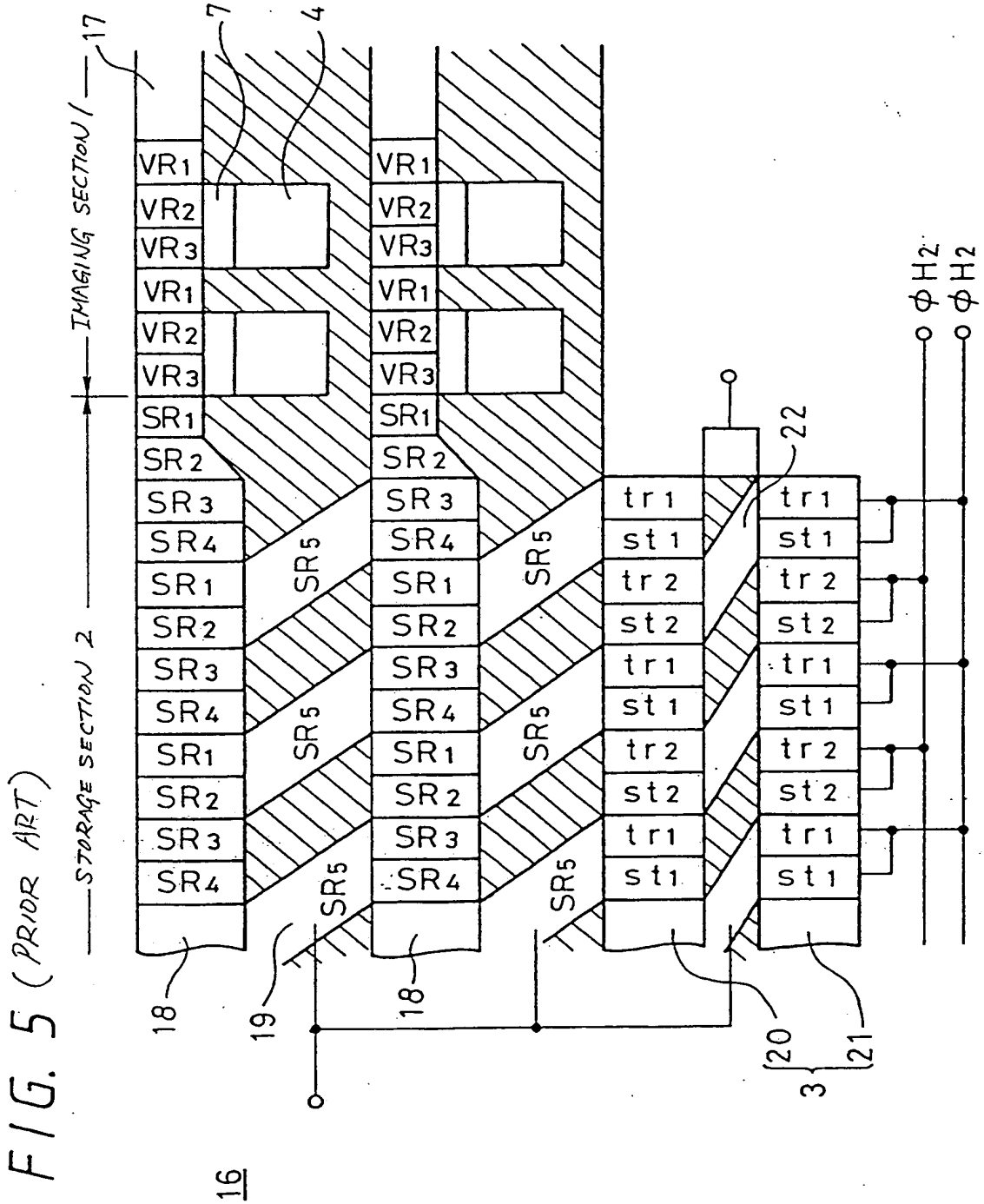


FIG. 5 (PRIOR ART)

Fig. 6 (prior art)

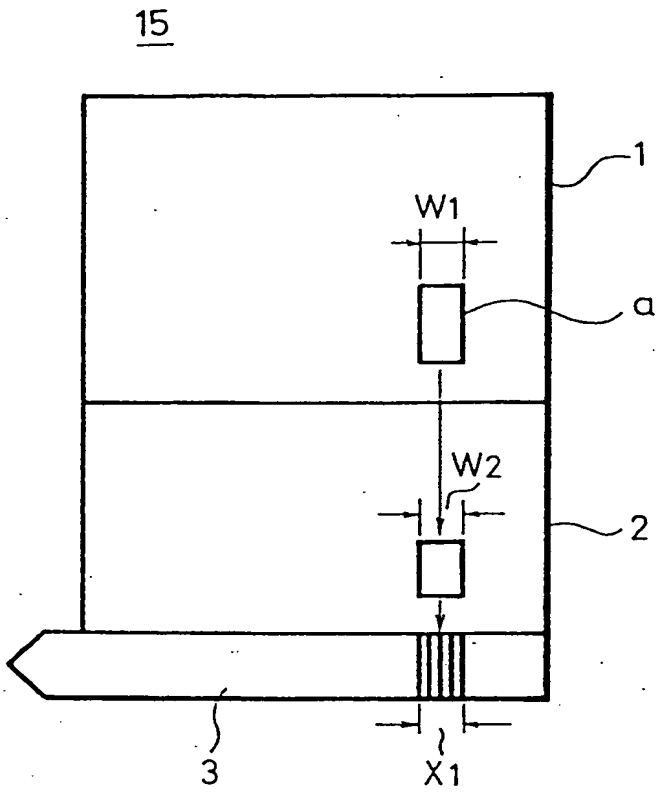
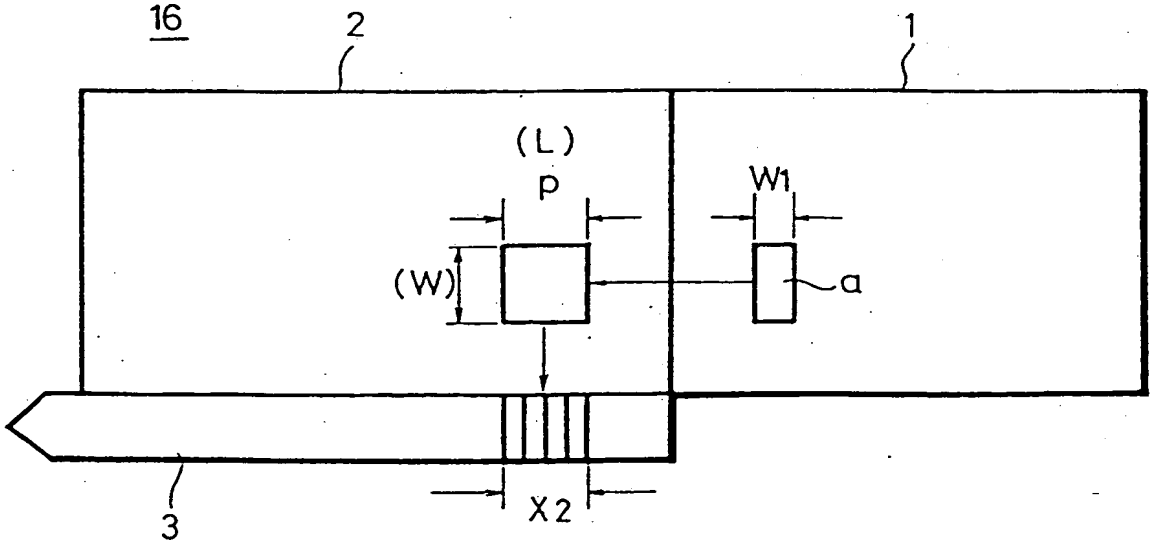


FIG. 7 (PRIOR ART)



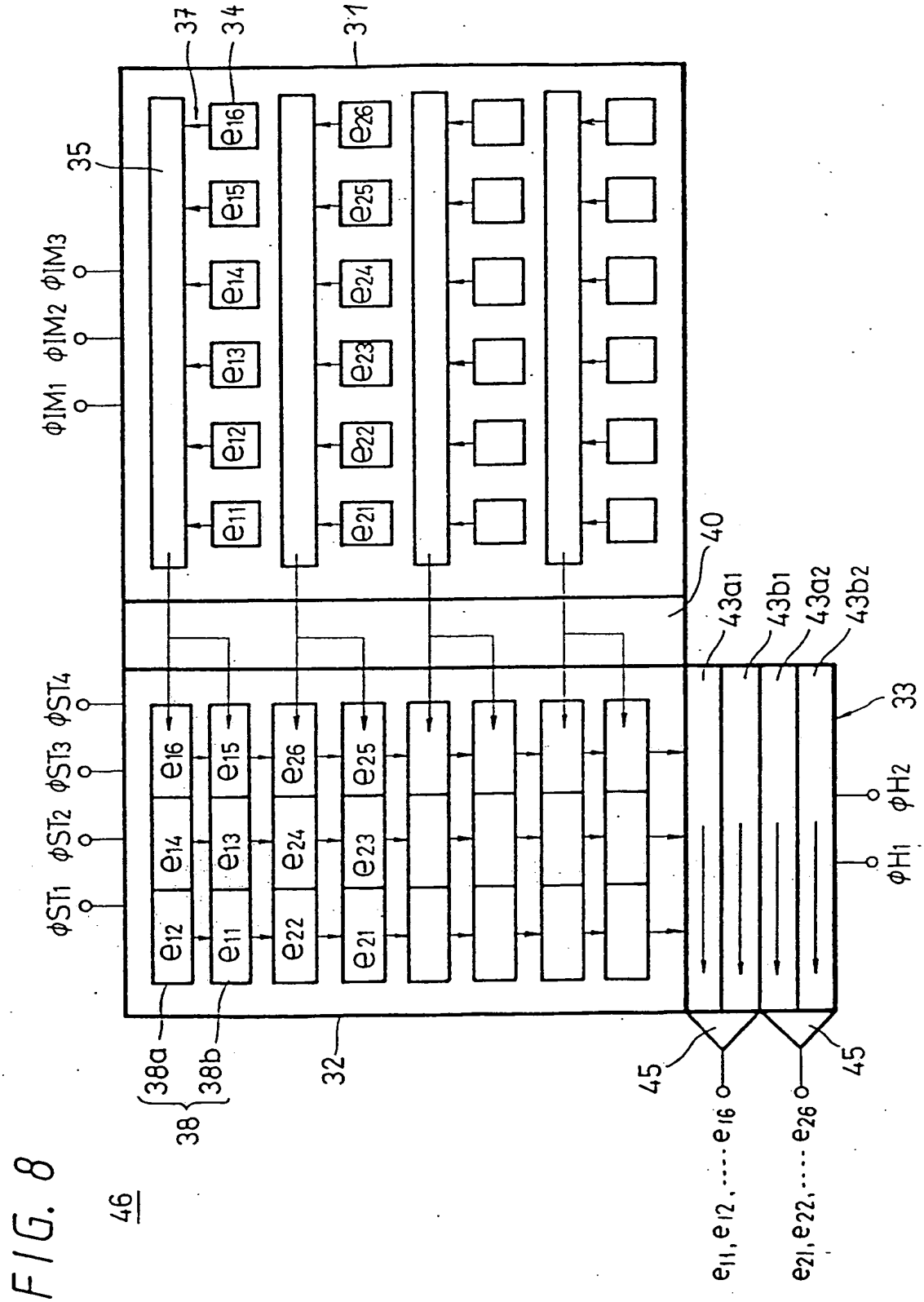

37
34
31
35
φIM1 φIM2 φIM3
e11 e12 e13 e14 e15 e16
e21 e22 e23 e24 e25 e26
40
43a1
43b1
43a2
43b2
33
φH1 φH2
φST1 φST2 φST3 φST4
38a
38b
38
32
45
45
e11, e12, ---- e16
e21, e22, ---- e26
46

FIG. 8

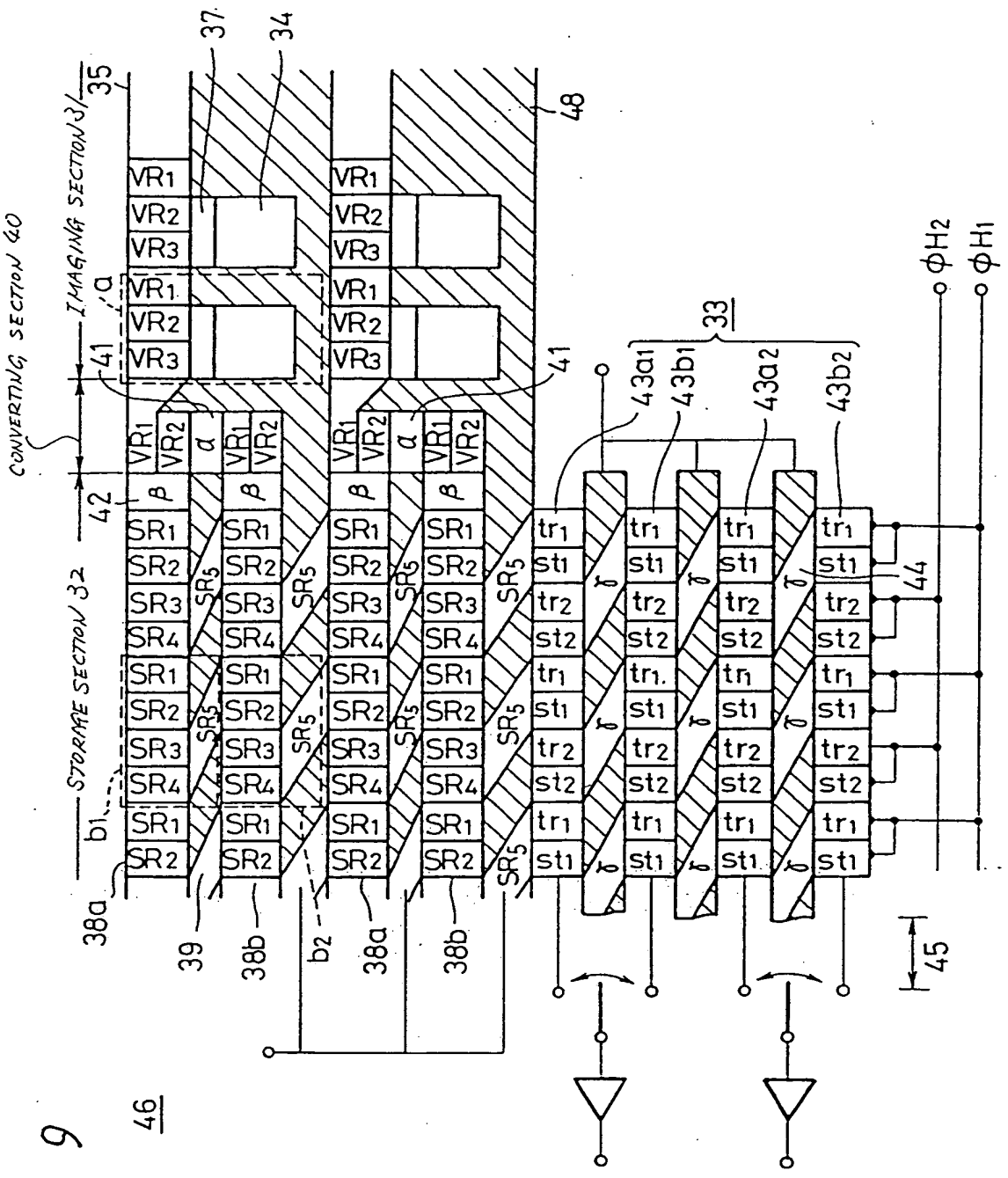
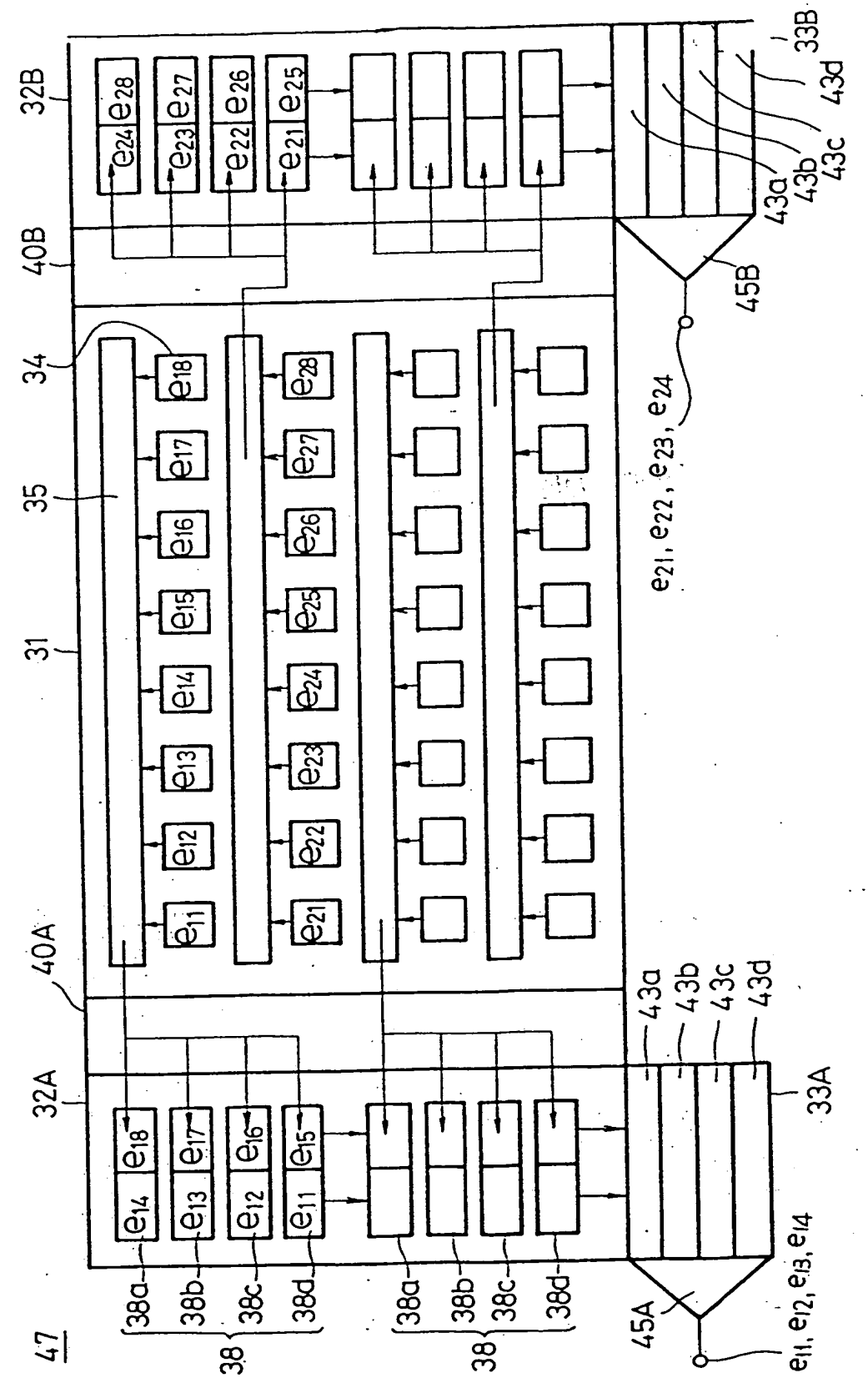

CONVERTING SECTION 40
IMAGING SECTION 31
STORAGE SECTION 32
35
37
34
48
41
42
VR1
VR2
VR3
α
β
SR1
SR2
SR3
SR4
SR5
38a
38b
39
b1
b2
33
43a1
43b1
43a2
43b2
tr1
tr2
st1
st2
γ
44
45
φH2
φH1
46

FIG. 9

FIG. 10


47
32A
32B
40A
40B
31
34
35
33A
33B
38
38a
38b
38c
38d
43a
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43c
43d
45A
45B
e11, e12, e13, e14
e21, e22, e23, e24
e11 e12 e13 e14 e15 e16 e17 e18
e21 e22 e23 e24 e25 e26 e27 e28

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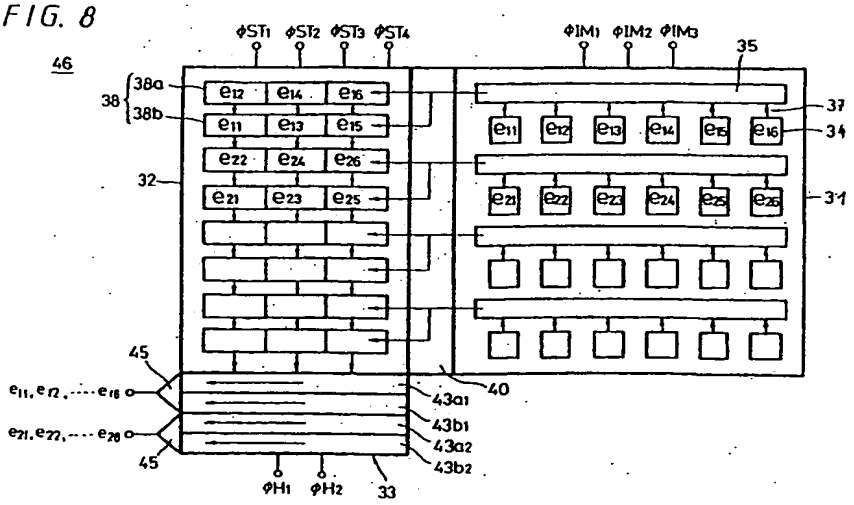
(54) **Fit type CCD image sensor.**

(57) A charge coupled device image sensor is comprised of an imaging section (31) including a plurality of photoelectric converting sections (34) arrayed in a matrix configuration for generating signal charges and a plurality of horizontal shift registers (35) arranged between the horizontal rows of the photoelectric converting sections (34) for transferring the signal charges via a readout section in the horizontal direction, a storage section having a plurality of horizontal shift registers (43a1...) for transferring the signal charges in the horizontal direction and in the vertical direction line by line, a readout section (33) coupled to the storage section and including a plurality of horizontal shift registers for reading out signal charges from the storage section, and a serial-to-parallel converting section (48) provided between the imaging section and the storage section for storing one-line of signal charges from the imaging section into double-line of image signal.

FIG. 8



EP 0 501 333 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 10 2935

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	PATENT ABSTRACTS OF JAPAN vol. 13, no. 277 (E-778)(3625) 26 June 1989 & JP-A-1 064 472 (TOSCHIBA CORP) 10 March 1989 * abstract *	1,2,5	H04N3/15
Y	PATENT ABSTRACTS OF JAPAN vol. 11, no. 31 (E-475)(2478) 29 January 1987 & JP-A-61 198 981 (CANON INC) 3 September 1986 * abstract *	1,2,5	
A	PATENT ABSTRACTS OF JAPAN vol. 11, no. 277 (E-538)(2724) 8 September 1987 & JP-A-62 077 768 (MATSUSHITA ELECTRONICS CORP) 9 April 1987 * abstract *	1	
A	US-A-4 737 841 (KINOSHITA ET AL.) * column 3, line 33 - line 61; figure 1 *	1	
P,A	EP-A-0 419 118 (SONY CORPORATION) * the whole document *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 JULY 1992	BEQUET T.P.

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